

REMARKS

Upon entry of the present amendment, claims 1-7 are pending in the present application. Claims 16-27 have been canceled previously. Claim 1 is amended herein, to more particularly point out and distinctly claim Applicants' invention, thus, for clarification purposes. This amendment is not considered to be a narrowing amendment.

Applicants submit herewith two Declarations Under 37 C.F.R. 1.132, both of which were submitted previously in the parent application, to which this application claims priority, U.S. Serial No. 09/525,247. These Declarations are relevant to the issues in the present application, and provide explanatory support for the distinction between the presently claimed invention and the prior art references cited in support of the rejection of Applicants' claims. Entry and consideration of these Declarations are respectfully requested. A more detailed description of the content of the Declarations, and the relevance and pertinence thereof to the present claims, is provided below.

Rejection of Claims 1-7 over Tashiro et al. in view of Hirohashi.

Claims 1-7 stand rejected as obvious over Tashiro et al., U.S. Patent No. 5,515,022, in view of Hirohashi, JP 6-112047). The Examiner asserted that

Tashiro et al. discloses a multi-layered chip inductor [1] comprising:

-at least one conductive pattern [31,32] having a thickness of 10 micro-meters or more and a width to thickness ratio from 1 to less than 5 [see column 6, lines 12-25];

-at least one pair of insulating layers [22,23] formed of magnetic material sandwiching the conductive pattern; and

-a thick conductor [35] connecting the conductive pattern.

Tashiro et al. discloses the instant claimed invention except for the inductor component being formed of a ceramic material.

Hirohashi discloses a ceramic chip inductor.

Thereupon, the Examiner concluded that it would have been obvious to use the inductor component of Tashiro et al. with a ceramic material as suggested by Hirohashi.

Applicants respectfully traverse this rejection, for at least the following reasons.

The Examiner has failed to identify all of the limitations of Applicants' claims in the cited prior art references. Specifically, the Examiner failed to identify where in either reference there is any teaching or suggestion that the insulation layers are actually in contact with the conductive pattern. The Examiner asserted only that the conductive pattern is "sandwiched between" the pair of insulating layers. This does not show the "in contact with" limitation of Applicants' claimed invention. Since the cited references fail to disclose all the limitations of Applicants' claimed invention, these references cannot be asserted to form the proper legal basis for a *prima facie* case of obviousness. Accordingly, the rejection should be withdrawn. Applicants respectfully request the Examiner to withdraw this rejection.

Both Tashiro et al. and Hirohashi disclose forming the conductive pattern by printing. As shown in detail in the herewith-submitted Declarations, forming a conductive pattern by printing results in formation of a specific gap between the conductive pattern and an insulation layer, which means the conductive pattern cannot be in contact with the pair of insulating layers. The specific gap of Tashiro et al. and Hirohashi is formed because the disclosed printing processes of the references necessarily use an ink or a paste formed from a binder and/or solvent and the

conductive material for printing in order to make the conductive material flowable for printing to the substrate. See., e.g., Tashiro et al., col. 8, lines 48-62. ("The conductor paste and the external electrode-forming paste are generally comprised of conductive particles, a binder and a solvent." (lines 60-62)). When the chip inductor is thereafter fired (at 850-950°C; see col. 9, line 13) to form the conductive pattern from the printing, the binder and solvent must be lost, resulting in a loss of volume as compared to the originally-applied material, and consequently resulting in formation of a specific, measurable gap between the conductive material and the overlying laminate. Thus, the conductive material and the insulation layer cannot be in contact, as claimed. Hirohashi also discloses that the conductive pattern is printed, so must also use a binder and/or carrier together with the conductive material in order to accomplish the disclosed printing. The two Declarations discussed below provide specific factual support for this argument, as discussed in detail below.

The Examiner failed to show this limitation, "interposing a conductive pattern between a pair of insulation layers so as to be in contact with the pair of insulation layers", of Applicants' claims in the cited references. Thus, the Examiner failed to state a legally correct *prima facie* case of obviousness.

Because all of the limitations of the claimed invention have not been shown, there can be no possible motivation to make the asserted combination, since doing so does not reach the presently claimed invention. Furthermore, because all of the limitations of the claimed invention have not been shown, there can have been no reasonable expectation of success in combining the disclosures of the cited references, since doing so does not reach the presently claimed invention. Thus, none of the three legally required elements of a *prima facie* obviousness case are present. Accordingly, for this reason, the rejections should be withdrawn.

Declarations of Eiichi Uriu.

The two Declarations Under 37 CFR 1.132 of Eiichi Uriu provide further factual support for the foregoing arguments and explanations. The Declarant, Mr. Eiichi Uriu, is one of the inventors of the presently disclosed and claimed invention. The First Declaration (dated March 7, 2002) includes details of experiments conducted by Mr. Uriu to observe the effects of producing conductive patterns by the electroforming process of the present invention and by the printing methods disclosed in Tashiro and Hirohashi. Results of these experiments are also detailed in the First Declaration. These results are discussed below in relation to specific features of the pending claims. These results demonstrate that the present invention would not have been obvious over these two references, since even if the references would be combined, the presently disclosed and claimed invention would not be obtained. The Second Declaration (dated 11 December 2002) provides additional explanation of terms used in the First Declaration.

No Specific Gap - "interposing a conductive pattern between a pair of insulation layers so as to be in contact with the pair of insulation layers"

Claim 1, and all of the claims dependent thereon, include the feature of the "interposing a conductive pattern between a pair of insulation layers so as to be in contact with the pair of insulation layers", i.e., there is no specific gap formed between the conductive pattern and the insulation layers. As shown in the following, the present invention results in the formation of the conductive pattern in contact with the insulation layers, but the prior art must form a specific gap due to the printing process used to form the conductive pattern. This "in contact with" feature distinguishes the claimed invention over the prior art.

First Declaration

Applicants' "interposing a conductive pattern between a pair of insulation layers so as to be in contact with the pair of insulation layers" feature of the present invention is a direct result of using an electroforming process as discussed in the First Declaration, in section 2, and would not be obtained by the methods of the cited references.

That is, as explained in section 2.2 of the First Declaration in the electroforming process of the present invention the step "interposing a conductive pattern between a pair of insulation layers so as to be in contact with the pair of insulation layers" results in the electroformed conductive pattern being formed with no subsequent size reduction. This is so because electroforming involves the formation of the pattern by metal plating, without the use of any constituent materials which could evaporate or otherwise decompose and become lost as a result of the sintering performed subsequently to cure the green sheets, such that no shrinkage of the conductive pattern occurs. Thus, these elements are "in contact with" each other. This "in contact with" is illustrated in Figure B (sample 2) on page 8 of the First Declaration.

On the other hand, the First Declaration also shows that in the printing methods of Tashiro and Hirohashi shrinkage of the conductive pattern necessarily results from the evaporation of the binder resin and the solvent in the conductive paste making up the conductive pattern as a result of the sintering. This shrinkage results in the formation of a specific gap between the conductive pattern and the pair of insulating layers. This gap is shown clearly in Fig. A (sample 1) on page 8 of the Declaration.

The First Declaration further explains (p. 7, 1st full paragraph) that such a specific gap renders the printed conductive pattern of Tashiro et al and Hirohashi susceptible to contaminants, such as water or plating solvent, which may become present in this gap and which can change the characteristics, such as the resistance

or impedance, of the printed conductive pattern, therefore changing the characteristics of the inductor formed using this printed conductive pattern.

Therefore, as shown by the facts set forth in the First Declaration, including the Figure A, even if a specific gap is not shown in the drawings of Tashiro and Hirohashi, such a gap must exist as a direct result of the printing methods used by Tashiro and Hirohashi. Thus, Tashiro and Hirohashi also do not teach or suggest the claimed invention in relation to the no specific gap feature thereof.

Accordingly, the invention of claims 1-7 would not have been obvious over the asserted combination of Tashiro and Hirohashi, since as shown by the Declaration of Mr. Uriu, even if these references were combined, they do not yield all of the features of the present invention, as specified in these claims.

Second Declaration

The Second Declaration was submitted in order to further explain some terms used in the First Declaration. Of specific interest here is the explanation relating to the "no specific gap" feature which is described in the present claims in the step of "interposing a conductive pattern between a pair of insulation layers so as to be in contact with the pair of insulation layers".

Paragraph 7 of the Second Declaration provides additional explanation of the "no specific gap" feature, i.e., the step of "interposing a conductive pattern between a pair of insulation layers so as to be in contact with the pair of insulation layers" feature of the presently claimed invention.

As stated in paragraph 7 of the Second Declaration:

The term "no specific gap" as in no specific gap between the conductive pattern and the insulation layers, means that the conductive pattern and the insulation layers are substantially in contact.

Here again, Applicants show that the presently claimed invention provides a conductive pattern and insulating layers in contact, which fully distinguishes the present claims over the cited references.

Thickness and Width to Thickness Ratio

Claims 1-7 further include the feature of the conductive pattern having a thickness of 10 μm or more and a width to thickness ratio from 1 to less than 5. Such a thickness and width to thickness ratio of the conductive pattern of the present invention is a direct result of using an electroforming process as discussed in the First Declaration in the last paragraph of section 1.2 and in section 2.2.

That is, as explained in the First Declaration, no shrinkage occurs in the electroformed conductive pattern, such that the width of 40 μm and thickness of 20 μm is achieved in the final inductor structure.

On the other hand, the First Declaration also shows that the above thickness and width conditions of the conductive pattern cannot be achieved by the printing methods of Tashiro and Hirohashi. That is, as explained in the Declaration, the printed conductive pattern first has a thickness of about 12 μm (which is a practical limit), however after sintering the thickness is reduced by about 40% to about 7 μm due to shrinkage.

Therefore, contrary to the disclosure in Tashiro that a thickness of 5-50 μm is possible, the declaration clearly shows that this is not the case in practice, where the final thickness is less than 7 μm . With a width of about 50 μm , the width to thickness ratio of the prior art is about 7 (i.e., 50 μm /7 μm \approx 7). Thus, Tashiro and Hirohashi do not teach or suggest the claimed invention in relation to the thickness (10 μm or more) and width to thickness ratio (1 to <5) features thereof.

A prerequisite for a case of obviousness is that the Examiner must show that the asserted combination of prior art references teach all of the limitations of the allegedly obvious claims. In the present case, the First Declaration of Mr. Uriu rebuts any such showing.

Furthermore, even though Tashiro et al. disclose thickness and widths (at col. 6, lines 15-17) which would arguably fall within Applicants' claimed range, in the Examples, Tashiro et al. show clearly that Applicants' claimed limitations would not be obtained. Specifically, in Example 1, Tashiro et al. lay down a conductive line have a width of 180 and a thickness of 10, which is in fact, a width to thickness ratio of 18. This is very far outside the claimed range of width to thickness ratio from 1 to less than 5. Example 2 was apparently carried out in the same manner as was Example 1, so it would be expected to have the same results in width to thickness ratio.

Accordingly, Applicants respectfully submit that for these additional reasons, claims 1-7 would not have been obvious over the asserted combination of Tashiro and Hirohashi, since as shown by the Declarations of Mr. Uriu, even if these references were combined, they do not include all of the limitations of the claimed invention.

For the foregoing reasons, Applicants respectfully submit that the presently pending claims patentably distinguish over the cited combination of references. The Examiner is respectfully requested to reconsider and withdraw the rejection of Applicants' claims.

Product by Process Claims

Applicants' claims are product by process claims, and therefore, under USPTO practice, the patentability of the claimed invention resides in the structure of the

product, not in process limitations. Thus, process limitations are normally not accorded patentable weight, except in a situation as in the present case in which the electroforming process necessarily results in the formation of a product which differs from the prior art products which are made by a different process. As shown herein, the structures are necessarily different. The facts to support this point are set forth in detail in the foregoing, including the two Declarations under 37 CFR 1.132 and the discussions above.

Request for Initialed Copies of Forms PTO-1449

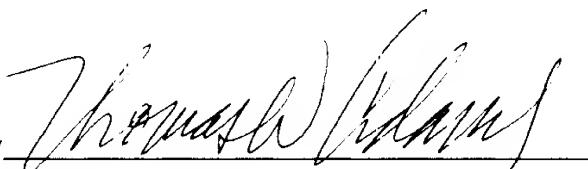
On January 31, 2003 and February 10, 2003, Applicants submitted supplemental Information Disclosure Statements. These IDS forms may have not reached the Examiner prior to his consideration of the application. Applicants request the Examiner to consider the references cited in these IDSs and to provide Applicants with an initialed copy of the forms PTO-1449 submitted therein.

In the event issues arise as a result of the filing of this paper, or remain in the prosecution of this application, Applicants request that the Examiner telephone the undersigned attorney to expedite allowance of the application. Should a Petition for Extension of Time be necessary for the present Reply to the outstanding Office action to be timely filed (or if such a petition has been made and an additional extension is necessary) petition therefor is hereby made and, if any additional fees are required for the filing of this paper, the Commissioner is authorized to charge those fees to Deposit Account #18-0988, Docket No. YAMAP0347USD.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, P.L.L.

Date: May 20, 2003

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